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A Study of Highly Scalable DG-FinDRAM

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***Abstract*—This letter reports the scalability of a capacitor-less 1T-DRAM, and proposes a new concept about extending the use of 1T-DRAM to gate lengths of less than 50 nm. Superior characteristics such as long retention time and large sense margin even for gate lengths around 50 nm can be obtained with a double-gate fully depleted FinFET DRAM. Considering capacity, speed, power, and structural complexity of embedded memory, the capacitor-less 1T-DRAM has the possibility of playing the leading role among other memories.**

***Index Terms*—Double-gate (DG) MOSFET, DRAM, embedded memory, FinFET, floating-body effect, silicon-on-insulator (SOI).**

I. Introduction

SEVERAL reports about a capacitor-less 1T-DRAM or floating-body cell (FBC), have been published recently [1]–[8]. This new memory cell uses a floating-body of a partially depleted (PD) silicon-on-insulator (SOI) MOSFET as a storage node. The cell senses whether the majority carriers (holes) accumulate in the floating-body as the threshold voltage ($V_{\rm th}$) changes. Therefore, the 1T-DRAM does not need a complicated storage capacitor, and this means that the cell has a good process compatibility with logic devices and can be made very small ($4F^2$). Although it is mentioned that the 1T-DRAM cell offers several advantages compared with conventional DRAMs, the research on scalability has not been discussed. In this paper, we report the scalability of a 1T-DRAM that utilize the floating-body effect in the PD-SOI MOSFET and proposes a new concept about extending the use of 1T-DRAM to gate lengths of less than 50 nm.

II. Scalability of 1T-DRAM

The retention time is a critical concern for DRAM scalability. When the gate length scales down, the channel impurity concentration increases in order to suppress short-channel effects. However, the increase in channel impurity concentration degrades the junction leakage characteristics, which leads to a lower storage charge in the capacitor and a shorter retention time. Similar phenomena occur in the case of 1T-DRAM. The body impurity concentration increases and the Si thickness decreases in order to avoid short-channel effects [9]. Therefore, the retention time becomes shorter due to the increasing leakage current at the body-source/drain junction. Fig. 1 simulates the relationship between body voltage and hold time with various body impurity concentrations. The initial state is "0," and gate and drain voltages are set to -1 and 0 V, respectively to hold the "0" state. The higher the body impurity concentrations are, the faster the body voltages change to the "1" state. This verifies that increasing the junction leakage current makes the "0" retention time shorter. Moreover, the number of storage charges decreases with gate length unlike the conventional 1T/1C DRAM, because of the reduced volume of the floating-body. This leads to a smaller sense margin. Consequently, it is difficult for a conventional 1T-DRAM cell, namely, a single-gate PD-SOI MOSFET to be scaled down to gate lengths less than 100 nm.

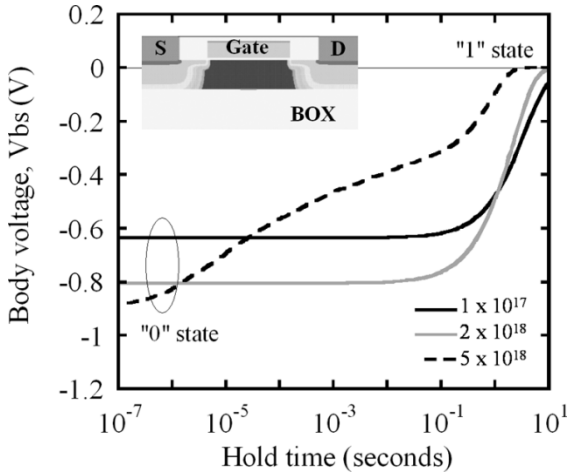

Fig. 1. Relationships between body voltage and "0" hold time. The inset is a 1T-DRAM used for the two-dimensional simulation. The L_g is 0.2 μm. The higher body concentration degrades the "0" retention due to the increasing leakage current.

III. DG FinFET DRAM

We believe that a double-gate fully depleted FinFET DRAM (DG-FinDRAM) can overcome the scalability issues for 1T-DRAM [10]. Fig. 2 shows schematic views of the DG-FinDRAM and summarizes typical bias conditions for the memory operation. Although a similar structure was proposed, it was used only for adjusting Vth [11]. The DG-FinDRAM uses the front MOS structure as a conventional switching transistor, and uses the back MOS structure to form the floating-body storage node. An appropriate reverse-biasing of the back MOS structure keeps excess holes in the body, which means that memory operations are possible even for highly scaled fully depleted FinFETs. The DG-FinDRAM uses the floating-body with very low impurity concentration, which leads to a reduced junction leakage current and a longer "0" retention time. It is obvious that the DG-FinDRAM is a robust structure for scaling.

To verify the effect of reverse biasing, the hole concentration was simulated for various back-gate voltages. Fig. 3 shows the time dependence of hole concentration at the back interface,

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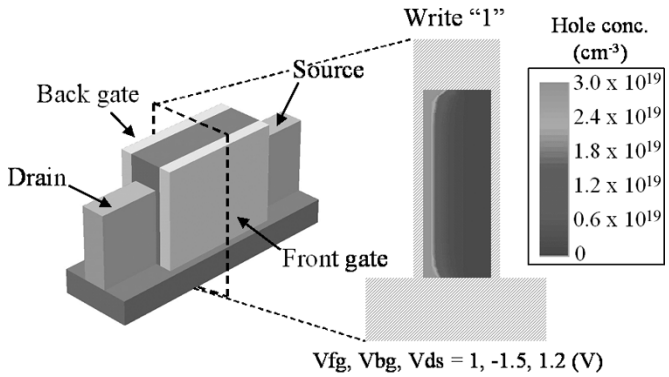

	Write "1"	Write "0"	Read	Hold
Gate voltage	1	1	0.8	-1
Drain voltage	1.2	-1	0.2	0
Back-gate voltage	-1.5	-1.5	-1.5	-1.5

Fig. 2. DG-FinDRAM structure used for 3-D simulation and typical bias conditions for the memory operation. The L_g is 50 nm. The fin thickness is 10 nm.

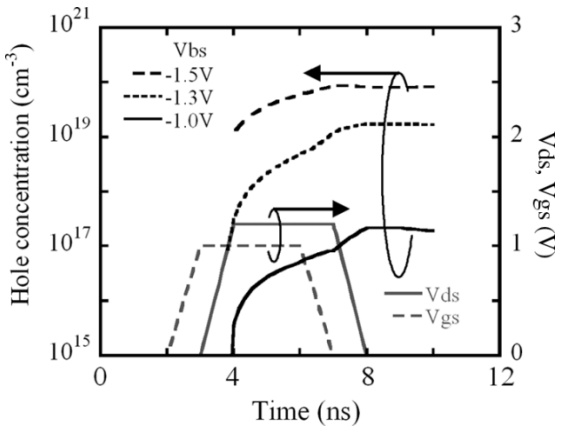

Fig. 3. Relationships between back-gate voltages and hole concentration in the Si fin. Holes were generated by impact ionization at drain edge. In this case, the $V_{\rm bs}$ of -1.5 V is necessary for memory operation.

during generation of excess holes by impact ionization and retention of them. Device parameters used for three–dimensional (3-D) simulation are as follows; L_g of 50 nm, fin thickness of 10 nm, gate oxide thickness of 1 nm, and body impurity concentration of 1×10^{16} cm^{-3}. The holes of more than 1×10^{19} cm-3 can be accumulated at the back interface for the $V_{\rm bs}$ of -1.5 V. As the $V_{\rm bs}$ of -1 V is too small to form a floating-body storage node, generated holes don't accumulate and flow into a source region. The DG-FinDRAM has a large sense margin as well, which is due to the large drain current (I_d) difference between states "1" and "0." Fig. 4 simulates the energy-band diagram and the corresponding I_d–V_g characteristics for states "1" and "0" of DG-FinDRAM. The DG-FinDRAM has a straight energy-band distribution in the Si fin, which causes a large $V_{\rm th}$ shift and a consequent large I_d difference with a small change in hole numbers at the back interface.

Fig. 5 shows a schematic top-down view of a 9F^2 DG-FinDRAM cell, which is a practical structure. For our

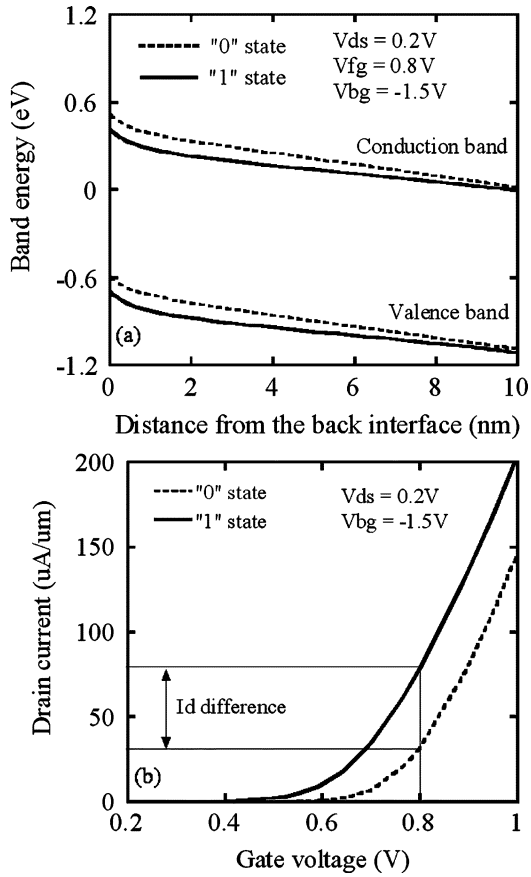

Fig. 4. (a) Energy-band diagram for "0" and "1" states in the Si fin. Band energy at the back interface is lower for "1" state due to the hole accumulation. (b) I_d–V_g characteristics of the DG-FinDRAM. The large I_d difference between "0" and "1" states leads to a large sense margin.

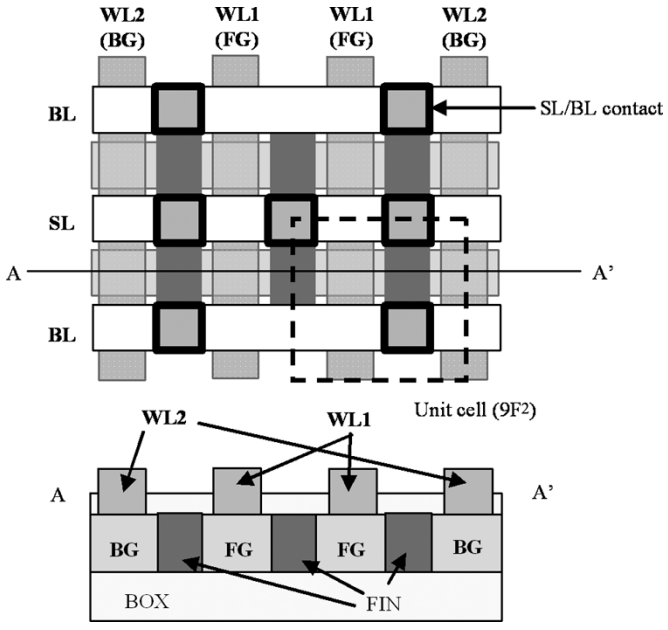

Fig. 5. Schematic top-down and cross-sectional views of the DG-FinDRAM cell (9F2).

DG-FinDRAM, minimum cell size of 4F^2 can be fabricated by using an additional metal layer and raised source/drain (S/D} structure. Although a planar asymmetric DG DRAM was

presented previously [12], it is rather difficult to fabricate a $4F^2$ cell size due to the longer back-gate electrode. Moreover, an overlap capacitance between the back-gate and S/D is added to the BL capacitance, which makes switching slower. Note that a fin width can be optimized for logic and memory respectively, which makes it easy to fabricate DRAM/Logic mixed chips.

IV. Conclusion

Considering capacity, speed, and structural complexity of embedded memory, a capacitor-less 1T-DRAM seems most promising. For the scalability of 1T-DRAM, the higher channel impurity concentration required to suppress short-channel effects significantly degrades retention characteristics. It is quite difficult for a conventional 1T-DRAM to scale down L_g to less than 100 nm. To overcome this problem, a DG FinFET DRAM was proposed. The DG-FinDRAM has a floating-body with a very low impurity concentration even at a gate length of 50 nm, which leads to a long retention time. Moreover, a large sense margin was obtained because of straight energy-band distribution. The DG-FinDRAM should thus be a very promising embedded memory when advanced MOSFETs like FinFETs come into use in the near-future technology nodes.

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